In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (canceled).

1 2. (currently amended) An automated method for designing an integrated circuit layout
2 with a computer, comprising:
3 (a) selecting a plurality of cells that are intended to be used in the integrated circuit
4 layout;
5 (b) determining ~~initial~~ delay values <u>for</u> ~~associated with~~ the <u>selected plurality of</u> cells <u>in</u>
6 <u>order to satisfy delay constraints</u> ~~prior to determining an initial placement of the cells~~; and
7 (c) performing ~~an initial~~ <u>a</u> placement of the <u>selected plurality of</u> cells <u>after determining</u>
8 <u>said delay values, the placement</u> including <u>assigning loads for the selected plurality of cells and</u>
9 <u>determining a</u> ~~an initial~~ size or area of the <u>selected plurality of</u> cells in response to the <u>said</u>
10 <u>assigned loads and said delay values</u> ~~initial placement~~.

1 3-4. (canceled).

1 5. (currently amended) The automated method of claim [[4]] <u>2</u> further comprising:
2 determining [[a]] <u>the</u> size or area of the cells that will approximately maintain ~~the~~
3 ~~adjusted~~ <u>said</u> delay values <u>determined prior to said placement</u>.

1 6. (canceled).

1 7. (previously presented) The automated method of claim 2 further comprising:
2 routing the digital circuit to generate the integrated circuit layout using a finalized size or
3 area of the selected plurality of cells.

1 8. (currently amended) The automated method of claim 2 wherein ~~the initial~~ <u>said</u> delay
2 values are determined using gain.

1   9. (currently amended) The automated method of claim 2 wherein ~~the initial~~ said delay

2   values are determined using logical effort.

1   10. (currently amended) The automated method of claim 2 wherein ~~the initial~~ said delay

2   values are determined by finding a preferred gain of the cells.

1   11. (previously presented) The automated method of claim 10 wherein the preferred gain

2   of the cells is determined using a continuous buffering assumption.

1   12. (currently amended) The automated method of claim 2 wherein ~~the initial~~ said delay

2   values are determined during library analysis.

1   13. (currently amended) The automated method of claim 2 wherein ~~the initial~~ said delay

2   values are determined using a typical load of the cells.

1   14. (previously presented) The automated method of claim 13 wherein the typical load is

2   determined based on gain considerations.

1   15. (previously presented) The automated method of claim 2 wherein the size or area of

2   the cells is variable and not fixed at the time the cells are selected.

1   16. (previously presented) An automated method for designing an integrated circuit

2   layout with a computer of a circuit specified by a netlist, comprising:

3   (a) providing a library of cells;

4   (b) determining initial delay values for a plurality of cells from said library of cells to be

5   used in the integrated circuit layout of the circuit before determining an initial size or area of the

6   cells, and using a timing driven covering method to map said plurality of cells to the circuit; and

7   (c) performing an initial placement of the cells, including assigning net lengths to nets on

8   the cells, and determining the initial size or area of the cells in response to the initial placement.

1   17. (previously presented) The automated method of claim 16, including

2   inserting buffers based on an estimation of area savings in the circuit prior to determining

3   said initial size or area of the cells.

1   18. (previously presented) The automated method of claim 16, including

2   compressing or stretching delay values associated with cells prior to determining said

3   initial delay values for the cells.

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